Amendments to the Claims

1. *(Currently Amended)* An electronic circuit, comprising a signal conductor ~~(11),~~ a power supply reference conductor ~~(10)~~ and a switching circuit coupled between the signal conductor ~~(11)~~ and the power supply reference conductor ~~(10)~~, the switching circuit comprising:

- a substrate arrangement ~~(100, 102)~~ coupled to the power supply reference conductor ~~(10);~~
- a first MOS transistor ~~(17)~~ realized on said substrate arrangement ~~(100, 102)~~ with a source, a drain and a gate, the source being coupled to the power supply reference conductor ~~(10),~~ the first MOS transistor ~~(17)~~ having a first conductivity type;
- a second MOS transistor ~~(18)~~ realized on said substrate arrangement ~~(100, 102)~~ with a source, a drain and a gate, the source being coupled to the drain of the first MOS transistor ~~(17),~~ the drain being coupled to the signal conductor ~~(11),~~ the second MOS transistor ~~(18)~~ having a second conductivity type opposite the first conductivity type;
- a control circuit ~~(13, 14, 15, 16)~~ with outputs coupled to the gate of the first MOS transistor ~~(17)~~ and the gate and source of the second MOS transistor ~~(18),~~ the control circuit ~~(13, 14, 15, 16)~~ being arranged to switch between an "on" state and an "off "state, in which the control circuit ~~(13, 14, 15, 16)~~ controls the gate source voltages of the first and second MOS transistor ~~(17, 18)~~ to make channels of these MOS transistors ~~(17, 18)~~ conductive and not to make the channels of these first and second transistors ~~(17, 18)~~ conductive respectively.

2. *(Currently Amended)* An electronic circuit according to claim 1, comprising a further power supply reference conductor ~~(12)~~ and a further switching circuit, complementary to the switching circuit, the further switching circuit comprising:

- a third MOS transistor ~~(27)~~ of the second conductivity type, having a source, a drain and a gate, the source being coupled to the further power supply reference conductor ~~(12);~~

- a second MOS transistor ~~(28)~~ of the first conductivity type, with a source, a drain and a gate, the source being coupled to the drain of the third MOS transistor ~~(27),~~ the drain being coupled to the signal conductor ~~(11)~~ or a further signal conductor ~~(202)~~;
- the control circuit ~~(13, 16, 19, 23, 26, 29)~~ having outputs coupled to the gate of the third MOS transistor ~~(27)~~ and the gate and source of the fourth MOS transistor ~~(28),~~ the control circuit ~~(13, 16, 19, 23, 26, 29)~~ applying gate source voltages to the third and fourth MOS transistor ~~(27, 28)~~ to make these third and fourth MOS transistors ~~(27, 28)~~ conductive and not to make these transistors conductive respectively.

3. *(Currently Amended)* An electronic circuit according to claim 2, wherein the control circuit ~~(13, 16, 19, 23, 26, 29)~~ is arranged to supply first substantially matching gate-source voltages to the first and fourth MOS transistor ~~(17, 28)~~ and second substantially matching gate-source voltages to the second and third MOS transistor ~~(18, 27).~~

4. *(Currently Amended)* An electronic circuit according to claim 1, wherein the control circuit comprises:
- a power supply input ~~(12)~~ for supplying a power supply voltage with a first polarity relative to the power supply reference conductor ~~(10),~~ the first conductivity type being such that the channel of the first MOS transistor ~~(17)~~ becomes conductive when a voltage at its gate has a second polarity, opposite the first polarity relative to its source;
- a pump circuit ~~(16)~~ fed with the power supply voltage and arranged to generate the gate voltage of the first MOS transistor with the second polarity relative to the power supply reference conductor ~~(10)~~ in the "on" state.

5. *(Currently Amended)* An electronic circuit according to claim 1, wherein the control circuit comprises:
- a power supply input ~~(12)~~ for supplying a power supply voltage relative to the power supply reference conductor ~~(10)~~ with a first polarity, the second conductivity type being such that the channel of the second MOS transistor becomes

conductive when a voltage at its gate has a second polarity, opposite the first polarity relative to its source;

- a resistive element ~~(15)~~ coupled between the gate and source of the second MOS transistor;
- a current source circuit ~~(14)~~ coupled between the power supply input and the gate of the second MOS transistor ~~(18),~~ for supplying a predetermined, state dependent current from the power supply input to through the resistive element ~~(15).~~

6. *(Currently Amended)* An electronic circuit according to claim 5, comprising a further resistive element ~~(370)~~ and a current mirror circuit ~~(372, 374)~~ with an input branch and an output branch, the further resistive element ~~(370)~~ and the input branch being coupled in series between the power supply reference conductor ~~(10)~~ and the further power supply reference conductor ~~(12),~~ the output branch being coupled to the gate of the second MOS transistor ~~(18),~~ an input/output factor of the current mirror and a ratio between resistance values of the resistive element ~~(376)~~ and the further resistive element ~~(370)~~ having values so that a first voltage drop over the further resistive element ~~(370)~~ is substantially equal to a second voltage drop over the resistive element ~~(376).~~

7. *(Currently Amended)* An electronic circuit according to claim 6, wherein the control circuit comprises:

- a pump circuit ~~(16)~~ fed with the power supply voltage and arranged to generate the gate voltage of the first MOS transistor with the first polarity relative to the power supply reference conductor in the "on" state, the pump circuit comprising junction type pumping diodes ~~(350, 352)~~, the current mirror comprising bipolar transistors ~~(372, 374).~~

8. *(Currently Amended)* An electronic circuit, comprising a signal conductor ~~(200),~~ a first and second power supply conductor ~~(10,12)~~, a first switching circuit coupled between the first power supply conductor ~~(10)~~ and the signal conductor ~~(200)~~ and a second switching circuit coupled between the second power supply conductor ~~(10)~~ and the signal conductor ~~(200)~~ or a further signal conductor ~~(202),~~ the first switching circuit comprising:

- a first PMOS transistor ~~(17)~~ with a source, a drain and a gate, the source being coupled to the first power supply conductor ~~(10;~~

- a first NMOS transistor ~~(18)~~ with a source, a drain and a gate, the source being coupled to the drain of the first PMOS transistor ~~(17)~~, the drain being coupled to the signal conductor ~~(11);~~

the second switching circuit comprising:

- a second NMOS transistor ~~(27)~~ with a source, a drain and a gate, the source being coupled to the second power supply conductor ~~(12);~~

- a second PMOS transistor ~~(28)~~ with a source, a drain and a gate, the source being coupled to the drain of the second NMOS transistor ~~(27)~~, the drain being coupled to the signal conductor ~~(11)~~ or the further signal conductor ~~(202);~~

the electronic circuit comprising:

- a control circuit ~~(13, 16, 19, 23, 26, 29)~~ with outputs coupled to the gate of the first PMOS transistor ~~(17),~~ the gate of the second NMOS transistor ~~(27),~~ the gate and source of the first NMOS transistor ~~(18)~~ and the gate and source of the second PMOS transistor ~~(28),~~ the control circuit ~~(13, 16, 19, 23, 26, 29)~~ being arranged to switch between an "on" state and an "off "state, in which the control circuit ~~(13, 16, 19, 23, 26, 29)~~ controls the gate source voltages of the first and second PMOS transistor ~~(17, 28)~~ and the first and second NMOS transistor ~~(18, 27)~~ to make channels of these transistors conductive and not to make the channels of these first and second transistors conductive respectively.

9. *(Currently Amended)* An electronic circuit according to claim 8, wherein the control circuit ~~(13, 16, 19, 23, 26, 29)~~ is arranged to supply first substantially matching gate-source voltages to the first and second PMOS transistor ~~(17, 28)~~ and second substantially matching gate-source voltages to the first and second NMOS transistor ~~(18, 27).~~